A Two-Stage Monolithic IF Amplifier Utilizing a Ta_2O_5 Capacitor

ALEJANDRO CHU, LEONARD J. MAHONEY, MICHAEL E. ELTA, MEMBER, IEEE, WILLIAM E. COURTNEY, M. C. FINN, WILLIAM J. PIACENTINI, AND JOSEPH P. DONNELLY, MEMBER, IEEE

Abstract — **A two-stage monolithic IF amplifier incorporating a sputtered Ta_2O_5 capacitor has been fabricated. The monolithic capacitor is based on a composite layer structure consisting of Au, Ta, Ta_2O_5, Ta, and Au. This layered structure is sequentially deposited in a single sputtering run, which eliminates particulate contamination. As a result, a thin pinhole-free dielectric layer can be deposited over large areas, and 140-pF capacitors have been fabricated with excellent yields. The large unit area capacitance of 1500 pF/mm^2 available with the present process has the potential for reducing the size of matching and bias circuits in microwave monolithic circuits and hybrid thin-film circuits.**

The monolithic amplifiers exhibit a gain of 17.5 ± 1.0 dB from 1.2 to 2.6 GHz and a minimum noise figure of $\sim$ 2.7 dB, with an associated gain of 17.5 dB at 1.7 GHz.

I. Introduction

Capacitors for Microwave Monolithic Circuits

A MONOLITHIC IF AMPLIFIER has been fabricated for use in a millimeter-wave heterodyne receiver chip [1]. The frequency range of the receiver goes from 1.2 to 2.8 GHz, which is determined by the bandwidth of the balanced mixer. Several monolithic multistage amplifiers in this frequency range have been fabricated using direct coupling or matching circuits, in which the blocking capacitor is also a component of the RF matching structure [2], [3], [4]. In contrast, the present design of the two-stage amplifier consists of two cascading gain units in a 50-Ω system using an interstage coupling capacitor. To maintain the series reactance of the blocking capacitor below 5 Ω, a capacitance of 40–80 pF is required. This requirement imposes a difficult fabrication problem because capacitors based on dielectric materials presently used in monolithic fabrication can achieve only modest values of capacitance per unit area. Typical values of specific capacitance obtained in the present work using 5000 Å of polyimide, SiO_2, or Si_3N_4 are 53, 70, and 132 pF/mm^2, respectively, as shown in Table I. Use of these low dielectric constant materials, for the fabrication of 60-pF interstage coupling capacitors, resulted in low yield because of the high probability of including pinholes in the large areas required. A solution to this problem is the use of a higher dielectric constant material, such as Ta_2O_5.

TABLE I
COMPARISON OF DIELECTRIC MATERIALS FOR THIN-FILM CAPACITORS COMPOSITION OF TANTALUM OXIDE FILMS

MATERIAL	RELATIVE DIELECTRIC CONSTANT	THICKNESS (Å)	CAPACITANCE (pF/mm^2)
POLYIMIDE	3	5000	53
SiO_2	4-5	5000	71
Si_3N_4	6-8	5000	132
ANODIZED Ta_2O_5	~27-30	~3000	834
THERMALLY OXIDIZED Ta_2O_5	~27-30	~2000	1251
REACTIVELY SPUTTERED Ta_2O_5	~27-30	~1750	1430

Anodized Ta_2O_5 capacitors with Ta anodes are utilized in silicon IC's. Specific capacitances in the range of 600 pF/mm^2 have been obtained [2], but high conductor losses in the Ta electrode limit operation to frequencies below 10 kHz. In 1968, LaChapelle [5] proposed the use of an Al underlayer to increase the conductivity of the bottom electrode. Using this approach, Pitetti and Worobey [6], [7] and later Feinstein and Pagano [8] have demonstrated higher operating frequencies to approximately 10 MHz. Although further improvements seem possible, the anodized Ta_2O_5 capacitor process using an Al underlayer is not compatible with Au-based metallization systems used in GaAs monolithic circuits.

In view of these limitations, we have developed a reactively sputtered Ta_2O_5 thin-film capacitor process that is compatible with monolithic integration of GaAs circuits and is capable of achieving specific capacitances of $\sim$ 1500 pF/mm^2. This value is over an order of magnitude higher than those obtained for polyimide, SiO_2, and Si_3N_4 capacitors.

II. High-Frequency Ta_2O_5 Capacitors

The Ta_2O_5 dielectric layer for use in the capacitor can be obtained by anodic oxidation [9] or thermal oxidation [10] of a Ta layer. Alternatively, Ta_2O_5 can be reactively sputtered [11], [12] from a Ta target by Ar ions in the presence of partial pressures of oxygen. Anodic oxidation

Manuscript received May 18, 1982. This work was supported by the Department of the Army.

A. Chu, L. J. Mahoney, W. E. Courtney, M. C. Finn, W. J. Piacentini, and J. P. Donnelly are with Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173

M. E. Elta was with Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173. He is now with the Electrical Engineering Department, University of Michigan, Ann Arbor, MI 48104

0018-9480/83/0100-0021$01.00 ©1983 IEEE

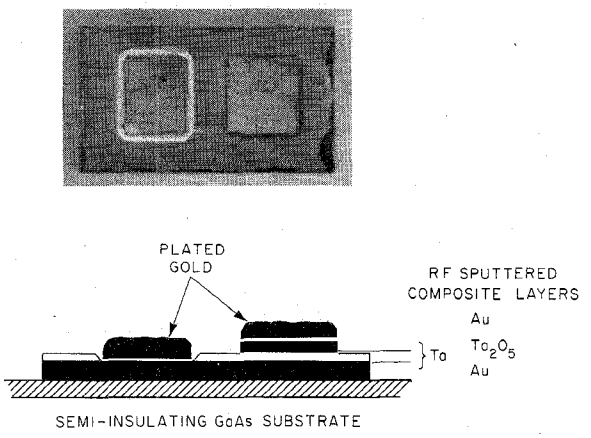


Fig. 1. High-frequency tantalum pentoxide capacitor.

TABLE II

DEPOSITION METHOD	O/Ta ATOMIC RATIO
THERMAL	2.49
ANODIZED	2.54
SPUTTERED	2.55

is performed in a 1:3:2 solution of oxalic acid, ethylene glycol, and water at 65°C under a potential of 75 V. Thermal oxidation is performed in oxygen or air at a temperature of 450°C, at a rate of 120 Å/min. The results of Auger analyses performed on the various types of Ta_2O_5 layers are summarized in Table II, which lists the atomic ratios of O to Ta obtained by using a standard of bulk Ta_2O_5. The data in Table II indicate that the layers obtained by the three techniques all have the composition Ta_2O_5 within experimental error. Typical values of specific capacitance obtained for each type of capacitor are shown in Table I. Dielectric thicknesses in the range of 1750–3000 Å reflect the practical range of thicknesses associated with each fabrication technique. The reactive sputter deposition technique produces the thinnest pinhole-free dielectric layers, therefore, yielding the largest specific capacitance of 1430 pF/mm^2.

A photograph of a high-frequency Ta_2O_5 capacitor is shown in Fig. 1. The top electrode measures 125 μm by 125 μm. The cross section of the capacitor shown below reveals a sequence of five layers: Au, Ta, Ta_2O_5, Ta, and Au. The Au layers are the top and bottom electrodes for the capacitor, the Ta_2O_5 layer is the dielectric, and the thin Ta layers serve the purpose of bonding the Ta_2O_5 to the Au. Without the Ta layer, adhesion of Ta_2O_5 to the Au would be poor. Thicknesses of the layers are 1250, 250, and 1750 Å for Au, Ta, and Ta_2O_5, respectively. To minimize losses, the Ta thickness should be kept to the minimum required for good adhesion.

In the reactively sputtered capacitor process all five

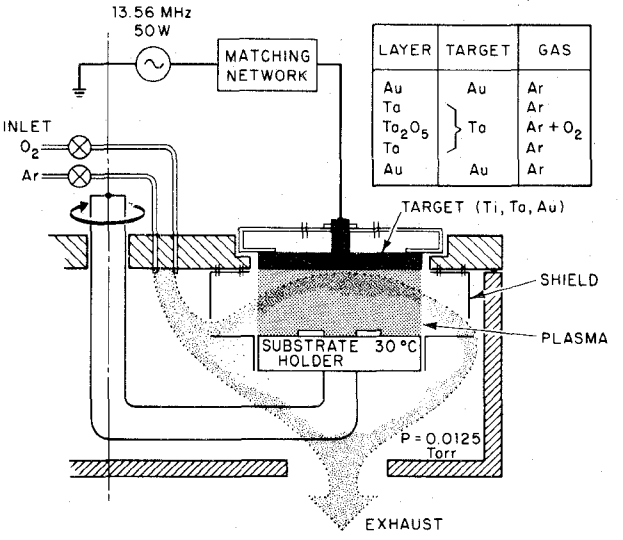


Fig. 2. Parallel-plate RF diode sputtering system for deposition of Au, Ta, and Ta_2O_5 layers.

layers are deposited sequentially in a single sputtering run without breaking vacuum. An important difference between this process and the oxidation processes is that wafer handling does not occur in the formation of the dielectric layer, so that particulate contamination is greatly reduced. The apparatus used for deposition of the composite layer is a RANDEX parallel-plate RF diode sputtering unit, as shown in Fig. 2. The initial Au and Ta layers are deposited from their respective targets in an Ar plasma at 50-W RF power. The flow rate of Ar is 20 sccm. Deposition of the Ta_2O_5 layer is accomplished by reactive sputtering of the Ta target using a mixture of 15 percent O_2 in Ar, with the RF power maintained at 50 W. The deposition rate of the Ta_2O_5 layer is 13 Å/min, compared to 50 Å/min for Ta. The rate is reduced because an oxide layer is formed on the Ta target, which is then sputter deposited more slowly by the Ar ions onto the substrate. The final Ta and Au layers are deposited under conditions described previously. Deposition times for the Au, Ta, and Ta_2O_5 are 6, 5, and 135 min, respectively.

Fig. 3 shows the result of Auger analysis performed on one of the composite films. The atomic concentration is plotted against sputtering time to display a depth profile of the film. The thick Au top electrode was etched off prior to Auger analysis to reduce sputtering time. The sharp transitions between layers and the uniformity of composition throughout the entire Ta_2O_5 layer demonstrates the potential of the reactive sputtering process for the deposition of thin layers in a reproducible way. The sputtering rate of each layer is determined from control samples of the respective materials. These rates are then used to calculate the thicknesses of the layers within the capacitor. By this procedure, the thicknesses of the Au, Ta, and Ta_2O_5 layers have been determined as 1250, 250, and 1750 Å, respectively. Unlike anodic Ta_2O_5 capacitors which are polar, with the Ta electrode as the anode [13], the sputtered Ta_2O_5 capacitors are nonpolar due to the symmetry of the composite structure. This feature simplifies the mask layout of circuits incorporating sputtered Ta_2O_5 capacitors.

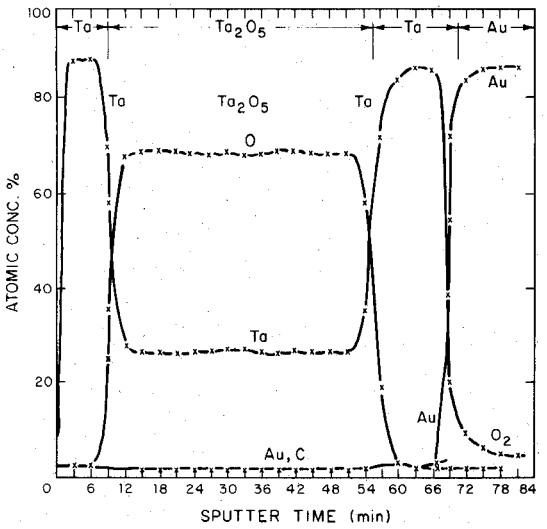


Fig. 3. Auger analysis of a sputtered Ta_2O_5 capacitor film showing the atomic concentration of Ta and Au as a function of sputtering time.

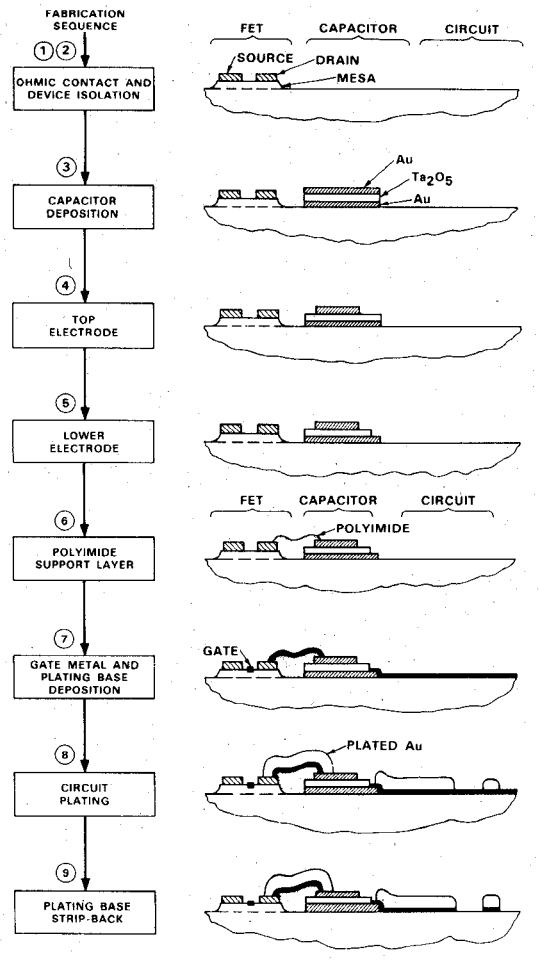


Fig. 4. Fabrication sequence of two-stage amplifier-incorporating Ta_2O_5 capacitor.

III. Fabrication Sequence of Two-Stage Amplifier

The fabrication sequence of the two-stage amplifier uses nine mask levels: three are associated with the fabrication of the capacitor, three which are used for the fabrication of FET's, and the remaining three levels which are for the fabrication of transmission lines and bias lines. Fig. 4 shows a diagram of the fabrication process. Wafer processing begins with the formation of the source and drain ohmic contacts of the FET's. In step 2, individual devices are isolated electrically by means of mesa etching. In step 3, the composite layers for the capacitor are sputter deposited and defined using a lift-off process. In step 4, the top Au layer is defined by wet etching and the underlying Ta layer defined by plasma etching. Although it was not implemented in the present case, trimming of capacitances could be incorporated at this step. In step 5, access to the bottom electrode of the capacitor is provided by etching the Ta_2O_5/Ta layers with a CF_4 plasma in a barrel type reactor. Etching was performed at a power level of 150 W and at a pressure of 2 torr. In step 6, a polyimide layer is defined to provide support for the connection to the top electrode of the capacitor. In step 7 the FET gates are formed by a lift-off process. The gate metal, which is based on a Au metallization system, serves several functions in the remainder of the fabrication. It is used as a plating base for transmission lines and connections to the capacitors, and in step 9 portions of gate metal in the field are protected during etching to leave bias lines on the circuit while unwanted areas are removed. Plating of transmission lines and bonding pads takes place in step 8.

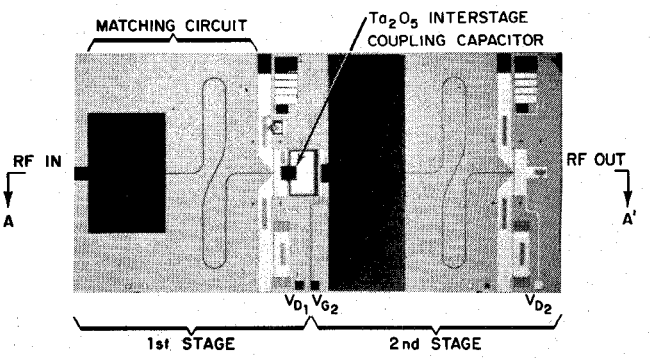


Fig. 5. Two-stage monolithic IF amplifier.

IV. Two-Stage IF Amplifier with Ta_2O_5 Interstage Coupling Capacitor

The reactively sputtered Ta_2O_5 capacitor described previously was integrated in the two-stage monolithic IF amplifier shown in Fig. 5. The capacitance was 140 pF and the area of the capacitor was 9.78×10^{-2} mm^2. This capacitance is about twice the desired value because the mask set was designed assuming a lower value of specific capacitance. The chip measures 2.5 mm by 5.0 mm. Input matching of the first-stage amplifier is provided by a pair of open-circuited 8-Ω stubs followed by a 140-Ω high-impedance line. Electrical lengths of the stub and transmission line at 2 GHz are 4.3 and 35.3°, respectively. The second stage of amplification is provided by a gain module previously described [1]. These modules can be cascaded with appropriate coupling capacitors at the 50-Ω level on input and output to give ~ 10 dB of gain per stage. Amplifiers of 20, 30, and 40 dB of gain have been fabricated by combining separate chips. The FET's have 1-μm by 500-μm gates

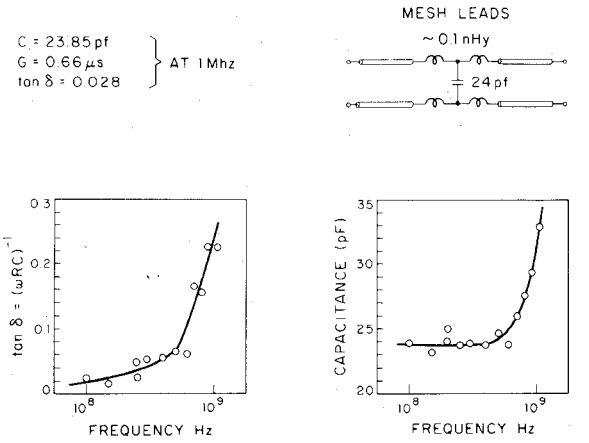


Fig. 6. Capacitance and loss tangent data from capacitors in shunt connection.

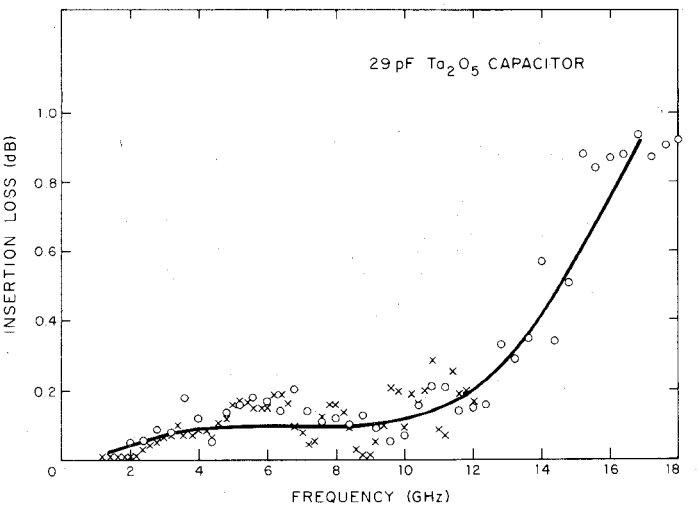


Fig. 7. Insertion loss as a function of frequency for a series connected 29-pF Ta_2O_5 capacitor. The circles and crosses refer to measurements made on two separate network analyzers.

positioned in a drain-to-source spacing of 5 μm. The channel formed by direct implantation of Se^+ ions in an undoped GaAs semi-insulating substrate. This differs from previous work [1], where the FET's were produced by vapor-phase epitaxial growth. At the present time the amplifier gain modules produced by epitaxial growth give 10-dB gain per module, 2 dB higher than the 8-dB gain obtained from modules produced by direct implantation into undoped substrates.

V. Electrical Test Results

Electrical evaluation of the reactively sputtered capacitors was performed with a 1-MHz capacitance bridge and with a network analyzer. Fig. 6 shows a comparison of the 1-MHz data with the network analyzer data obtained from the capacitor connected in shunt between two sections of microstrip lines. Agreement of the data is good to approximately 300 MHz. Values of the capacitance and loss tangent are ~ 24 pF and ~ 0.03, respectively. Divergence of the data at 1 GHz is an artifact of the resonance between the discrete capacitor and the inductance associated with the bonding wire used to connect the capacitor to the microstriplines and to ground. Fig. 7 shows the insertion loss as a function of frequency for a 29-pF Ta_2O_5 capacitor connected in series between two microstrip lines. The circles and crosses refer to measurements on two separate automatic network analyzers. The data shows an insertion loss of 0.1 dB$\pm$0.1 dB from 1 to 10 GHz. Evaluation of the capacitor as an interstage coupling capacitor was performed on a 140-pF capacitor, which was cut out from an actual monolithic two-stage amplifier. Test results show an insertion loss less than 0.15 dB at frequencies below 4 GHz.

The monolithic amplifiers were mounted in test fixtures and measured using a network analyzer and a noise figure measurement system. The noise figure circles at 1.7 GHz are shown in Fig. 8 and indicate a minimum noise figure of 2.5 dB. When the amplifier is connected to a 50-Ω source, the noise figure is 2.7 dB at 1.7 GHz, of which 1 dB is the contribution from losses in the high-impedance line. The associated gain is 17.5 dB. The bandwidth of the IF amplifier is shown in Fig. 9. The unit exhibits a gain in excess of 16.5 dB from 1.0 to 2.8 GHz. As previously mentioned, this is less than the 20 dB expected from previous amplifiers which were fabricated by using epitaxial growth.

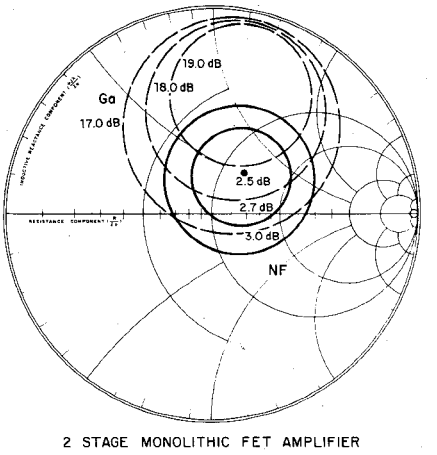


Fig. 8. Noise figure and gain circles in the input plane at 1.7 GHz.

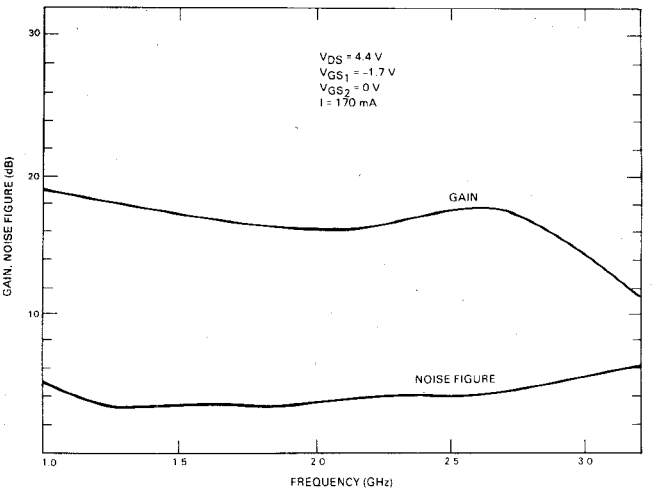


Fig. 9. Gain and noise figure of two-stage IF amplifier.

VI. Discussion

Integration of the two-stage amplifier with a 6-dB conversion loss balanced mixer [1] as a 31-GHz heterodyne receiver should provide an overall conversion gain above 10 dB. The 17.5-dB gain of the IF amplifier is sufficient to suppress noise contributions from additional stages, establishing the receiver noise figure.

Losses in the capacitor arise primarily from RF losses in the electrodes, rather than in the dielectric material. Therefore, higher Q's can be achieved by increasing the thickness of the electrodes and reducing the area of capacitors to produce capacitances consistent with circuit design requirements and safe fabrication limits. In the present application, the Au layers can be increased to $\sim$ 2000 Å and the area of the interstage coupling capacitor can be reduced by 50 percent and still achieve an adequate series reactance.

The reactively sputtered Ta_2O_5 capacitor, in addition to being necessary for the two-stage monolithic IF amplifier, may be useful for other monolithic circuits because large capacitances can be achieved with small size and high fabrication yield. Since coupling and bypass capacitors occupy a considerable fraction of the area in most microwave monolithic circuits, the large specific capacitance of the present capacitor can reduce the size and cost of both monolithic as well as thin-film hybrid circuits.

Acknowledgment

The authors wish to thank M. W. Pierce, K. M. Molvar, and J. J. Lambert for their technical expertise in the fabrication of the monolithic circuits, C. C. Snuggs for his contribution on ion implantation, and J. S. Gatley and J. H. Reinold for their assistance in the design of the mask set. Special thanks are due to R. V. Gray for discussions on the anodization of Ta and to R. T. Cerretani for his expertise on reactive sputtering. The authors are also indebted to R. W. Sudbury and R. A. Murphy for many technical discussions.

References

[1] A. Chu, W. E. Courtney, and R. W. Sudbury, "A 31-GHz monolithic GaAs mixer preamplifier circuit for receiver applications," *IEEE Trans. Electron Devices*, vol. ED-28, no. 2, pp. 149–154, Feb. 1981.

[2] D. P. Hornbuckle and R. L. Van Tuyl, "Monolithic GaAs direct coupled amplifiers," *IEEE Trans. Electron Devices*, ED-28, no. 2, pp. 175–182, Feb. 1981.

[3] W. C. Petersen, D. R. Decker, A. K. Gupta, J. Dully, and D. R. Ch'en, "A monolithic GaAs 0.1 to 10 GHz amplifier," in *1981 IEEE MTT-S Int. Microwave Theory Tech. Symp. Dig.*, pp. 354–355, June 1981.

[4] K. B. Niclas and R. R. Pereira, "Performance characteristics of lossy match vs. feedback amplifiers in *S* and *C* band," in *1982 IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 1982, pp. 196–197.

[5] E. A. LaChapelle, U.S. Patent 3 387 952, June 11, 1968.

[6] R. C. Pitetti and W. Worobey, U.S. Patent 3 671 825, June 20, 1972.

[7] ——, "Low density tantalum film capacitors with an aluminum underlay," in *Proc. IEEE 21st Electron. Comp. Conf.*, May 1971, pp. 195–197.

[8] F. L. Feinstein and R. Pagano, "Ta thin-film capacitors with an Al underlay for high-frequency applications," *IEEE Trans. Components, Hybrids Manufact. Tech.*, vol. CHMT-4, pp. 140–147, Mar. 1981.

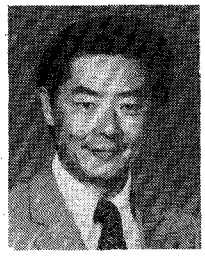
[9] W. D. Westwood, N. Waterhouse, and P. S. Wilcox, *Tantalum Thin Films*. New York: Academic Press, 1976, p. 290.

[10] L. Holland, *Vacuum Deposition of Thin Films*. London, England: Chapman & Hall, Ltd., 1966, ch. 15, pp. 450–455.

[11] T. M. Reith, "The reactive sputtering of tantalum oxide," Ph.D. dissertation, Syracuse University, Syracuse, NY, (University Microfilms Int., Ann Arbor, MI) 1980.

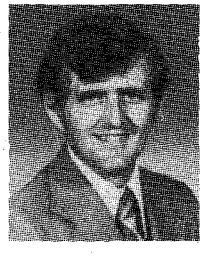
[12] M. E. Elta, A. Chu, L. J. Mahoney, R. T. Cerrentani, and W. E. Courtney, "Tantalum oxide capacitors for GaAs monolithic integrated circuits," *IEEE Electron Device Lett.*, vol. EDL-3, pp. 127–129, May 1982.

[13] R. W. Berry, P. M. Hall, and M. T. Harris, *Thin Film Technology*. New York: Van Nostrand, 1968, p. 522.



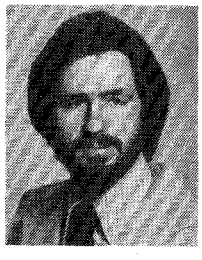
Alejandro Chu received the B.Sc., degree in 1970, and the M.Sc. and the E.E. degrees in 1972, all in electrical engineering, from the Massachusetts Institute of Technology, Cambridge. He received the Ph.D. degree from Stanford University, Stanford, CA, in 1977. His dissertation was in the field of ion implantation.

From 1972 to 1978, he worked at the Hewlett–Packard Company on the development of a wide-band 2–18 GHz sweeper and microwave components, such as YIG-tuned oscillators, frequency multipliers, and wide-band amplifiers. In 1975, he joined the Hewlett–Packard Technology Center where he was responsible for the characterization of GaAs FET's and later for the fabrication of GaAs integrated circuits. He has been a member of the technical staff at Lincoln Laboratory, MIT, Lexington, MA, since 1978. He is presently involved with the development of GaAs devices and monolithic circuits for a millimeter-wave transceiver. He is interested in the development of processing techniques adaptable for mass production.



Leonard J. Mahoney was born in Norwood, MA on October 7, 1944. He graduated from Wentworth Institute, Boston, MA, in 1964. He received the A.A. and B.A. degrees (with honors) in mechanical engineering from Northeastern University, Boston, MA, in 1973 and 1975, respectively.

He joined Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA, in 1972, where he has worked on the fabrication of a number of microwave devices including GaAs IMPATT diodes, surface-oriented mixer diodes, and FET's. He is currently an Assistant Staff Member in the Microelectronics Group working on process development and fabrication of GaAs IC's for millimeter-wave applications.



Michael E. Elta (S'75–M'78) was born in Flint, MI, on January 1, 1951. He received the B.S.E. degree in electrical engineering from General Motors Institute, Flint, MI, in 1975 and the M.S.E. degree in electrical engineering from The University of Michigan, Ann Arbor, in 1975. He completed a dissertation for the Ph.D. degree in electrical engineering at The University of Michigan, Ann Arbor, in 1978.

From 1969 to 1973 he was a cooperative engineering student at AC Spark Plug, GMC. Flint, MI, and at the University of Michigan he was a Research Assistant in the Electron Physics Laboratory from 1975 to 1978. From 1978 to 1982 he was a member of the research staff in the microelectronics group at MIT Lincoln Laboratory, Lexington, MA. At present he is an Assistant Professor in the Electrical and Computer Engineering Department at The University of Michigan, Ann Arbor, MI. He held a General Motors Fellowship for the academic year of 1973–1974 and a Rackham Predoctoral Fellowship for the academic year of 1977–1978. His research interests include semiconductor device physics, microelectronic fabrication, process modeling, and microwave device design.

Dr. Elta is a member of Tau Beta Pi, Sigma Xi, and the American Vacuum Society.

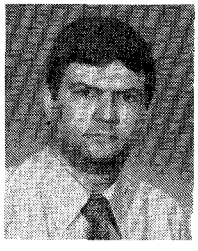
William E. Courtney was born in Lurgan, County Armagh, Northern Ireland, on October 3, 1936. He received the B.Sc. degree (with honors) in physics, and the Ph.D. degree in electrical engineering from the Queen's University of Belfast, Belfast, Northern Ireland, in 1959 and 1963, respectively.

From 1963 to 1966, he was a Department of Scientific and Industrial Research and Ministry of Aviation Post-Doctoral Research Fellow in the Department of Electrical Engineering, University of Leeds, England. From 1966 to 1968, he was a Post-Doctoral Fellow in the Centre for Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, and is presently a member of the Experimental Systems Group of Lincoln Laboratory, MIT, Lexington, MA.

✤

M. C. Finn, photograph and biography not available at the time of publication.

✤



William J. Piacentini was born in Boston, MA, on March 2, 1945. He received the B.S.E.E. and M.S.E.E. degrees from Northeastern University, Boston, MA, in 1976 and 1980, respectively.

He joined Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA, in 1968. After serving in the U.S. Army at Yuma Proving Ground, AZ, and in Vietnam, he returned to Lincoln Laboratory in the Space Communications Division where he was involved with low-noise millimeter-wave GaAs Schottky-barrier diodes for the LES-8/9 satellite communications system. Since 1976, he has been with the Solid-State Division where he is responsible for automated testing, characterization, and modeling of GaAs microwave devices.

✤

Joseph P. Donnelly (S'60–M'63) was born in Brooklyn, NY, in 1939. He received the B.S.E.E. degree from Manhattan College, Bronx, NY, in 1961 and the M.S. and Ph.D. degrees in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in 1962 and 1966, respectively. From 1965 to 1966, he was a NATO Post-Doctoral Fellow at Imperial College, London, England. His thesis work dealt with the electrical and photovoltaic properties of Ge–GaAs and Ge–Si heterojunctions grown by both liquid-phase and vapor-phase epitaxy.

While at Imperial College, he worked on developing a liquid-phase epitaxial system for the III–V compounds. In 1967, he joined the staff of Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA, where he has since been concerned with the device applications of ion implantation in the III–V, II–VI, and IV–VI semiconductor compounds. In the early 1970's, he worked primarily on developing ion-implantation technology for fabricating infrared detectors in the Pb-salts and InSb. More recently, his major interests have been in GaAs, InP, and related compounds. In this area, he has contributed both to the development of ion-implantation technology for the III–V semiconductors and the demonstration of its use in the fabrication of a wide variety of microwave and electrooptical devices. He is currently involved in the development of laser diodes, detectors, and modulators for high-speed optical communications.

Dr. Donnelly was a National Lecturer for the IEEE Electron Devices Society in 1979. He is an associate member of Sigma Xi.